

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

TRANSLATION
PCT

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

(PCT Rule 43bis.1)

		Date of mailing (day/month/year)
Applicant's or agent's file reference 04NPCT008		FOR FURTHER ACTION See paragraph 2 below
International application No. PCT/JP2005/005544	International filing date (day/month/year) 25.03.2005	Priority date (day/month/year) 25.03.2004
International Patent Classification (IPC) or both national classification and IPC		
Applicant NEC CORPORATION		

1. This opinion contains indications relating to the following items:

<input checked="" type="checkbox"/>	Box No. I	Basis of the opinion
<input type="checkbox"/>	Box No. II	Priority
<input type="checkbox"/>	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
<input type="checkbox"/>	Box No. IV	Lack of unity of invention
<input checked="" type="checkbox"/>	Box No. V	Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
<input checked="" type="checkbox"/>	Box No. VI	Certain documents cited
<input type="checkbox"/>	Box No. VII	Certain defects in the international application
<input type="checkbox"/>	Box No. VIII	Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/JP	Authorized officer
Facsimile No.	Telephone No.

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Box No. I	Basis of this opinion
1.	With regard to the language, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item. <input type="checkbox"/> This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rule 12.3 and 23.1(b)).
2.	With regard to any nucleotide and/or amino acid sequence disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of: a. type of material <input type="checkbox"/> a sequence listing <input type="checkbox"/> table(s) related to the sequence listing b. format of material <input type="checkbox"/> in written format <input type="checkbox"/> in computer readable form c. time of filing/furnishing <input type="checkbox"/> contained in the international application as filed. <input type="checkbox"/> filed together with the international application in computer readable form. <input type="checkbox"/> furnished subsequently to this Authority for the purposes of search.
3.	<input type="checkbox"/> In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
4.	Additional comments:

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Box No. V	Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement																			
<p>1. Statement</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%; padding: 5px;">Novelty (N)</td> <td style="width: 60%; padding: 5px;">Claims <u>2-5, 7-10</u></td> <td style="width: 20%; padding: 5px;">YES</td> </tr> <tr> <td></td> <td><u>1, 6, 11</u></td> <td>NO</td> </tr> <tr> <td style="padding: 5px;">Inventive step (IS)</td> <td style="padding: 5px;">Claims <u>2-5, 9</u></td> <td style="padding: 5px;">YES</td> </tr> <tr> <td></td> <td><u>1, 6-8, 10-11</u></td> <td>NO</td> </tr> <tr> <td style="padding: 5px;">Industrial applicability (IA)</td> <td style="padding: 5px;">Claims <u>1-11</u></td> <td style="padding: 5px;">YES</td> </tr> <tr> <td></td> <td><u></u></td> <td>NO</td> </tr> </table> <p>2. Citations and explanations:</p> <p>Document 1: JP 2002-305282 A (Shinko Electric Industries Co Ltd), 18 October 2002 Document 2: JP 5-109977 A (Mitsubishi Electric Corp), 30 April 1993 Document 3: JP 5-048001 A (Fujitsu Ltd), 26 February 1993 Document 4: JP 5-129516 A (Hitachi Ltd), 25 May 1993 Document 5: JP 11-163251 A (Matsushita Electronics Corp), 18 June 1999 Document 6: JP 5-075014 A (Fujitsu Ltd), 26 March 1993 Document 7: JP 2000-243906 A (Sharp Inc), 08 September 2000</p> <p>Claims 1, 6, and 11 The inventions of claims 1, 6, and 11 do not appear to possess novelty over document 1 cited in the ISR. Document 1 does not clearly describe "at least one semiconductor chip is supplied at least one power source and ground from the interposer substrate via the through wire." However, in the chip stacked semiconductor device described in document 1, electrical connections are only performed via through wires, and therefore at least one power source and ground are supplied via the through wires.</p> <p>Claim 8 The invention of claim 8 does not appear to involve an inventive step over document 1 cited in the ISR. Document 1 does not describe a "spacer provided above a first semiconductor chip, comprising a plurality of second through wires." However, spacers comprising through wires are commonly known, and a person skilled in the art could easily conceive of adopting this constitution.</p> <p>Claim 7 The invention of claim 7 does not appear to involve an inventive step over document 2 and document 3 cited in the ISR. The semiconductor device described in documents 2-3 has a structure in which a second semiconductor chip, comprising a circuit face on a bottom surface, is provided above a first semiconductor chip. Accordingly, a person skilled in the art could easily conceive of adopting the "interposer substrate" and "spacer" described in document 3 in the semiconductor device described in document 2.</p>			Novelty (N)	Claims <u>2-5, 7-10</u>	YES		<u>1, 6, 11</u>	NO	Inventive step (IS)	Claims <u>2-5, 9</u>	YES		<u>1, 6-8, 10-11</u>	NO	Industrial applicability (IA)	Claims <u>1-11</u>	YES		<u></u>	NO
Novelty (N)	Claims <u>2-5, 7-10</u>	YES																		
	<u>1, 6, 11</u>	NO																		
Inventive step (IS)	Claims <u>2-5, 9</u>	YES																		
	<u>1, 6-8, 10-11</u>	NO																		
Industrial applicability (IA)	Claims <u>1-11</u>	YES																		
	<u></u>	NO																		

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Box No. VI	Certain documents cited		
1. Certain published documents (Rule 43bis.1 and 70.10)	Application No. Patent No.	Publication date (day/month/year)	Filing date (day/month/year)
	JP 2004-152810 A	27.05.2004	28.10.2002
	[E, X]		
2. Non-written disclosures (Rule 43bis.1 and 70.9)	Kind of non-written disclosure	Date of non-written disclosure (day/month/year)	Date of written disclosure referring to non-written disclosure (day/month/year)

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Box V. 2

Claim 10

The invention of claim 10 does not appear to involve an inventive step over documents 2-5 cited in the ISR. The semiconductor device described in documents 2-5 has a structure in which a second semiconductor chip, comprising a circuit face on a bottom surface, is provided above a first semiconductor chip. Accordingly, a person skilled in the art could easily conceive of applying the "plurality of wires for each semiconductor chip supplying a power source and a ground" described in documents 4-5 to the semiconductor device described in document 2.

Claims 2-5 and 9

The inventions of claims 2-5 and 9 appear to involve an inventive step with respect to the documents cited in the ISR. Documents 6-7 do not describe a "second semiconductor chip provided with a plurality of through wires" or that "at least one power source and ground are supplied from an interposer substrate to a circuit face of a second semiconductor chip via thick film wires."